1. A whole chip electrostatic discharge, ECD, first embodiment circuit comprising:

a PN diode whose p-side connects to the input / output, I/O pad to be protected and whose N-side is connected to Vcc supply voltage,

a PMOS FET plus NMOS FET 2-device input stage connected between Vcc and Vss,

a resistor plus NMOS FET first mid stage connected between Vcc and Vss (ground),

a resistor to ground second mid-stage, and

a PMOS FET plus NMOS FET output stage connected between Vcc and Vss (ground) whose input connects from the mid stages and whose output drives an unused I/O pad.

2. The whole chip ESD protection circuit of claim 1 wherein said input stage contains said PN diode whose P-side is connected to the I/O pad to be protected and whose N-side is connected to Vcc.

3. The whole chip ESD protection circuit of claim 1 wherein said input stage contains said p-channel metal oxide semiconductor field effect transistor PMOS FET whose source is connected to Vcc and is common to the N-side of said PN diode, whose drain is connected in common with the p-side of said PN diode,

and to the drain of said NMOS FET in the input stage, and whose gate is connected to said mid stage circuit.

4. The whole chip ESD protection circuit of claim 1 wherein said input stage contains said n-channel metal oxide semiconductor field-effect transistor NMOS FET whose source is connected to Vss or ground, whose drain is connected in common with said p-side of said PN diode and in common with said I/O pad to be protected and in common with said drain of said PMOS FET in said input stage, and whose gate is connected to said mid stage circuit.

5. The whole chip ESD protection circuit of claim 1 wherein said first mid-stage contains an NMOS FET whose source is connected to ground, whose drain is connected to said gate of said PMOS FET of said input stage and is connected to said resistor of this 1st mid stage and is connected to said output stage.

6. The whole chip ESD protection circuit of claim 1 wherein said first mid-stage contains a resistor connected between said VCC power supply and said drain of said NMOS FET.

7. The whole chip ESD protection circuit of claim 1 wherein said second mid-stage contains a resistor connected between Vss or ground and between the gate of said NMOS FET in said first mid-stage, the gate of said NMOS FET of said first stage, and which is connected to the input of said output stage.

8. The whole chip ESD protection circuit of claim 1 wherein said output stage contains said PMOS FET whose source is connected to Vcc, whose drain is connected to an unzapped I/O pad, and to the drain of said NMOS FET in the output stage, and whose gate is connected to said gate of said PMOS FET in said input stage and connected to said drain of said NMOS FET in said input stage.

9. The whole chip ESD protection circuit of claim 1 wherein said output stage contains said NMOSFET whose source is connected to Vss or ground, whose drain is connected to an unzapped I/O pad and connected to said drain of said PMOS FET in said output stage and whose gate is connected to said NMOS FET of said input stage and to one side of said resistor in said 2nd mid-stage and connected to said gate of said NMOS FET of said first mid-stage.

10. The whole chip ESD protection circuit of claim 1 wherein several said first embodiment circuits (one for each I/O pad) are tied in parallel between Vcc and ground, in order to sink large ESD charge and current.

11. The whole chip ESD protection circuit of claim 1 wherein a drain to source intrinsic capacitor, Cds, of said NMOS FET in said input stage is used to couple charge from said zapped I/O pad to said input to said output stage.

12. The whole chip ESD protection circuit of claim 1 wherein said charge coupled through said intrinsic capacitance, Cds, of said NMOS FET of said input stage charges up an intrinsic capacitance, Cgs, of said NMOS FET of said output stage.

13. A whole chip electrostatic discharge, ECD, second embodiment circuit comprising:

a PN diode whose p-side connects to the input / output, I/O pad to be protected and whose N-side is connected to Vcc supply voltage,

a PMOS FET plus NMOS FET 2-device input stage connected between Vcc and Vss,

a resistor plus NMOS FET first mid stage connected between Vcc and Vss (ground),

a second mid-stage containing a second NMOS FET connected between input stage and ground, and

a PMOS FET plus NMOS FET output stage connected between Vcc and Vss (ground) whose input connects from the mid stages and whose output drives an unused I/O pad.

14. The whole chip ESD protection circuit of claim 13 wherein said input stage contains said PN diode whose P-side is connected to the I/O pad to be protected and whose N-side is connected to Vcc.

15. The whole chip ESD protection circuit of claim 13 wherein said input stage contains said p-channel metal oxide semiconductor field effect transistor PMOS FET whose source is connected to Vcc and is common to the N-side of said PN diode, whose drain is connected in common with the p-side of said PN diode, and to the drain of said NMOS FET in the input stage, and whose gate is connected to said mid stage circuit.

16. The whole chip ESD protection circuit of claim 13 wherein said input stage contains said n-channel metal oxide semiconductor field-effect transistor NMOS FET whose source is connected to Vss or ground, whose drain is connected in common with said p-side of said PN diode and in common with said I/O pad to be protected and in common with said drain of said PMOS FET in said input stage, and whose gate is connected to said mid stage circuit.

17. The whole chip ESD protection circuit of claim 13 wherein said first mid-stage contains an NMOS FET whose source is connected to ground, whose drain is connected to said gate of said PMOS FET of said input stage and is connected to said resistor of this 1st mid stage and is connected to said output stage.

18. The whole chip ESD protection circuit of claim 13 wherein said first mid-stage contains a resistor connected between said VCC power supply and said drain of said NMOS FET.

19. The whole chip ESD protection circuit of claim 13 wherein said second mid-stage contains an NMOS FET whose drain is connected to said gate of said NMOS FET in said first mid-stage, whose source is connected to Vss or ground, and whose gate is connected to said gate of said PMOS FET of said first stage.

20. The whole chip ESD protection circuit of claim 13 wherein said output stage contains said PMOS FET whose source is connected to Vcc, whose drain is connected to an unzapped I/O pad, and to the drain of said NMOS FET in the output stage, and whose gate is connected to said gate of said PMOS FET in said input stage and connected to said drain of said NMOS FET in said input stage.

21. The whole chip ESD protection circuit of claim 13 wherein said output stage contains said NMOSFET whose source is connected to Vss or ground, whose drain is connected to an unzapped I/O pad and connected to said drain of said PMOS FET in said output stage and whose gate is connected to said NMOS FET of said input stage and to the drain of said NMOS FET of said 2nd mid-stage and connected to said gate of said NMOS FET of said first mid-stage.

22. The whole chip ESD protection circuit of claim 13 wherein several said first embodiment circuits (one for each I/O pad) are tied in parallel between Vcc and ground, in order to sink large ESD charge and current.

23. The whole chip ESD protection circuit of claim 13 wherein a drain to source intrinsic capacitor, Cds, of said NMOS FET in said input stage is used to couple charge from said zapped I/O pad to said input to said output stage.

24. The whole chip ESD protection circuit of claim 13 wherein said charge coupled through said intrinsic capacitance, Cds, of said NMOS FET of said input stage charges up an intrinsic capacitance, Cgs, of said NMOS FET of said output stage.

25. A whole chip electrostatic discharge ECD method comprising the steps of:

connecting all input/output, I/O pads to each other with double isolation, and

inserting a circuit of the first embodiment of this invention between each adjacent I/O pair on a semiconductor chip.

26. The whole chip ECD method of claim 25 further comprising the steps of:

including a PN diode whose p-side connects to the input / output, I/O pad to be protected and whose N-side is connected to Vcc supply voltage,

including a PMOS FET plus NMOS FET 2-device input stage connected between Vcc and Vss,

including a resistor plus NMOS FET first mid stage connected between Vcc and Vss (ground),

including a resistor to ground second mid-stage, and

including a PMOS FET plus NMOS FET output stage connected between Vcc and Vss (ground) whose input connects from the mid stages and whose output drives an unused I/O pad.

27. A whole chip electrostatic discharge ECD method comprising the steps of:

connecting all input/output, I/O pads to each other with double isolation, and

inserting a circuit of the second embodiment of this invention between each adjacent I/O pair on a semiconductor chip.

28. The whole chip ECD method of claim 27 further comprising the steps of:

including a PN diode whose p-side connects to the input / output, I/O pad to be protected and whose N-side is connected to Vcc supply voltage,

including a PMOS FET plus NMOS FET 2-device input stage connected between Vcc and Vss,

including a resistor plus NMOS FET first mid stage connected between Vcc and Vss (ground),

including an NMOS FET in a second mid-stage connecting both the input stage and the output stage, and

including a PMOS FET plus NMOS FET output stage connected between Vcc and Vss (ground) whose input connects from the mid stages and whose output drives an unused I/O pad.